UNIVERSAL PARTS SEMICONDUCTOR

UP40N06

60V N-Channel Enhancement Mode MOSFET

DESCRIPTION

The UP40N06 is N channel enhancement mode power effect transitor which is produced using high cell density advanced trench technology.

The high density process is especially able to minize on-state resistance.These devices are. especially suited for low voltage application power management DC-DC converters.

FEATURE

60V/40 A, $R_{DS(ON)}$=16mΩ (typ.)@VGS= 10V

Super high design for extremely low $R_{DS(ON)}$

Exceptional on-resistance and Maximum DC current capability

Full RoHS compliance

TO252 package design

100% UIS Tested

100% Rg tested

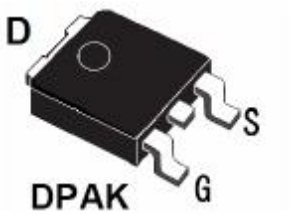
APPLICATIONS

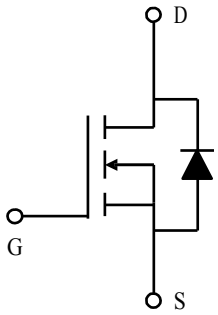
Power Management

DC/DC Converter

Load Switch

PIN CONFIGURATION





Copyright ®UNIVERSAL PARTS(HK)CO.,LTD

PART NUMBER INFORMATION

UP40N06AA-BB C	A= Package Code T: TO-252 BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product P: Pb free

ORDERING INFORMATION

Part Number	Package Code	Package	Shipping
UP40N06AT-TRG	T	TO-252	2500EA / T&R

※ Year Code : 0~9
※ Week Code : A~Z(1-26); a~z(27~52)
※ G : Green Product. This product is RoHS compliant.

ABSOLUPE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter	Max.	Units
VDS	Drain-to-Source Voltage	60	V
VGS	Gate-to-Source Voltage	± 20	
ID @ TA = 25°C	Continuous Drain Current, VGS @ 10V	35	A
ID @ TA = 70°C	Continuous Drain Current, VGS @ 10V	30	
ID @ TC(Bottom) = 25°C	Continuous Drain Current, VGS @ 10V	40	
ID @ TC(Bottom) = 100°C	Continuous Drain Current, VGS @ 10V	35	
ID @ TC = 25°C	Continuous Drain Current, VGS @ 10V (Package Limited)	40	
IDM	Pulsed Drain Current	90	
PD @TA = 25°C	Power Dissipation	2.1	W
PD @TC(Bottom) = 25°C	Power Dissipation	20	
	Linear Derating Factor	0.03	W/°C
TJ TSTG	Operating Junction and Storage Temperature Range	-55 to + 150	℃

Note: Absolupe maximum ratings are those values beyond which the device could be permanently damaged.
Absolupe maximum ratings are stress rating only and functional device operation is not implied

Copyright ®UNIVERSAL PARTS(HK)CO.,LTD

ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= 250uA	1.0		3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 48V, V_{GS}=0			1	uA
		V_{DS}= 48V, V_{GS}=0 T_J=85℃			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}= 10V, I_D= 40 A		16	18	mΩ
		V_{GS}= 4.5V, I_D= 36 A		18	22	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S= 1 A, V_{GS}=0V		0.7	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}= 30V V_{GS}= 10V I_D= 12 A		9		nC
Q_{gs}	Gate-Source Charge			1.6		
Q_{gd}	Gate-Drain Charge			1.8		
C_{iss}	Inpup Capacitance	V_{DS}= 30V V_{GS}=0V f=1MHz		540		pF
C_{oss}	Ouppup Capacitance			74		
C_{rss}	Reverse Transfer Capacitance			34		
$T_{d(on)}$	Turn-On Time	V_{DS}= 30V I_D= 5A V_{GEN}= 10V R_G=3.0		6		nS
T_r				4.6		
$T_{d(off)}$	Turn-Off Time			22		
T_f				4		

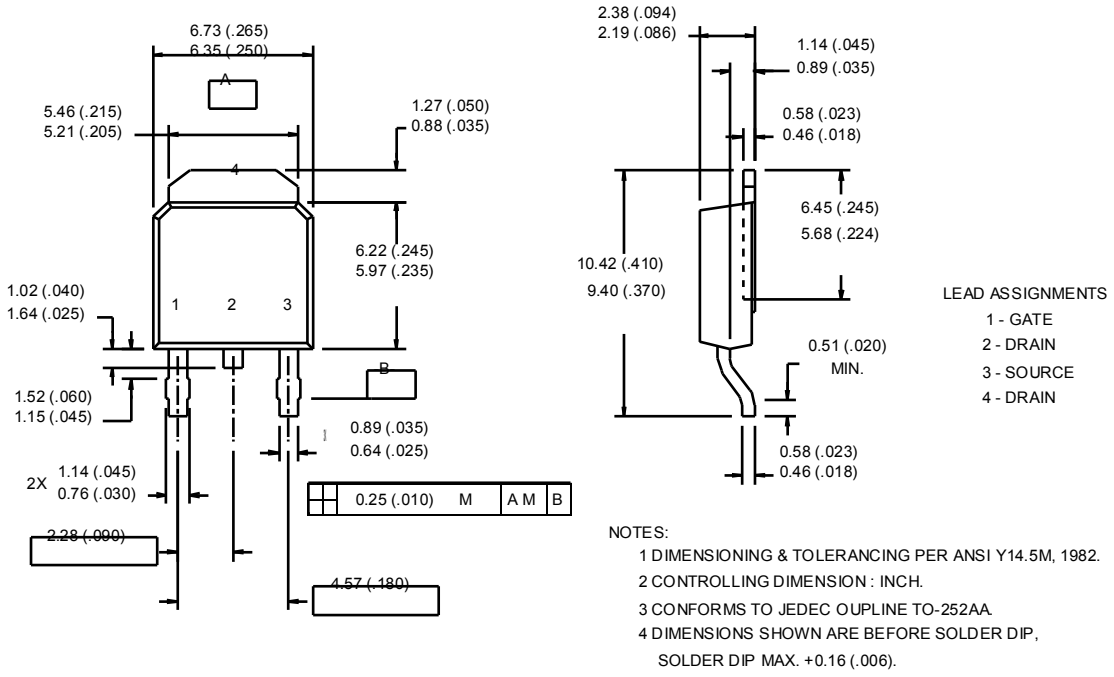
Note: 1. Pulse test: pulse width<=300uS, dupy cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

Copyright ®UNIVERSAL PARTS(HK)CO.,LTD

TO-252 Oupline Package Dimension

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

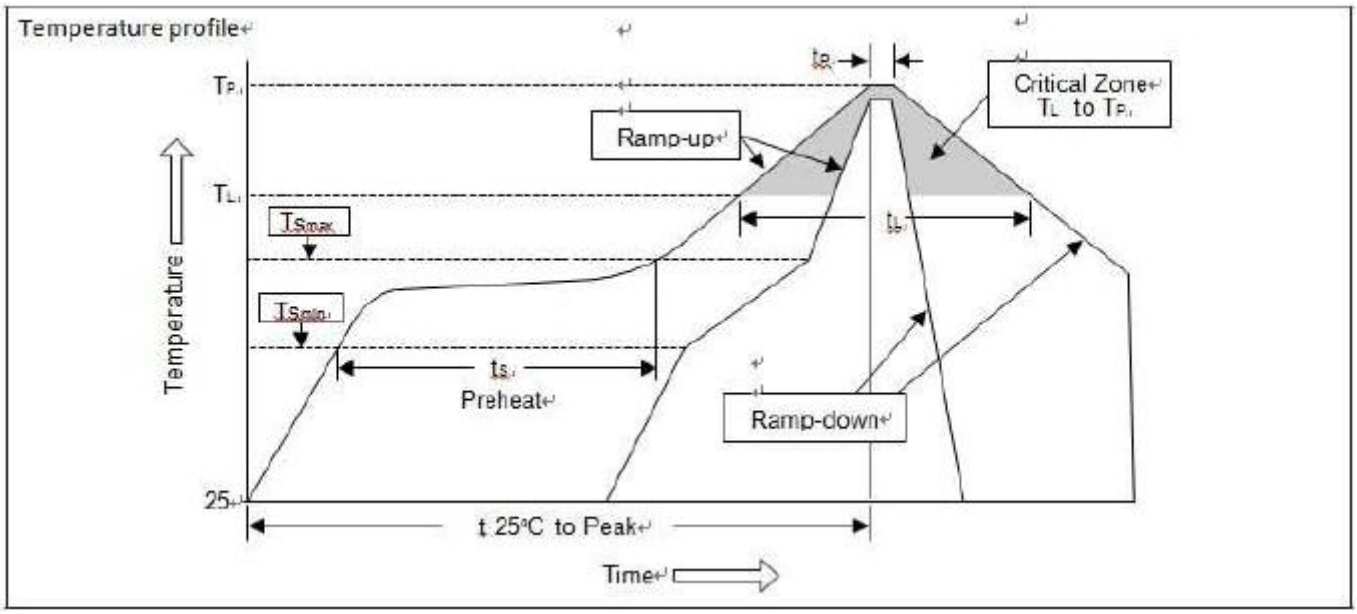
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUPLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Copyright ®UNIVERSAL PARTS(HK)CO.,LTD

SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eupectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minupes	<6 minupes

Copyright ®UNIVERSAL PARTS(HK)CO.,LTD

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5 ℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precaupions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Copyright ®UNIVERSAL PARTS(HK)CO.,LTD