UNIVERSAL PARTS SEMICONDUCTOR

up8726

30V N-Channel Enhancement Mode MOSFET

DESCRIPTION

The up8726 is N channel enhancement mode power effect transitor which is produced using high cell density advanced trench technology.

The high density process is especially able to minize on-state resistance.These devices are. especially suited for low voltage application power management DC-DC converters.

FEATURE

30V/85A, $R_{DS(ON)}$=3.0mΩ (typ.)@VGS= 10V

30V/65A, $R_{DS(ON)}$=4.5mΩ (typ.)@VGS= 4.5V

Super high design for extremely low $R_{DS(ON)}$

Exceptional on-resistance and Maximum DC current capability

Full RoHS compliance

TO-252 package design

100% UIS Tested

100% Rg tested

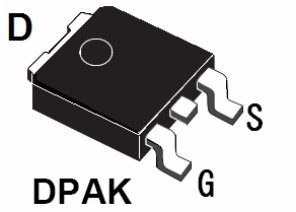
APPLICATIONS

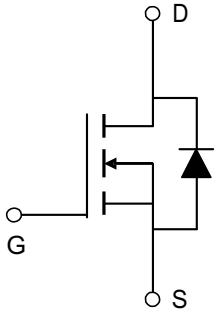
Power Management

DC/DC Converter

Load Switch

PIN CONFIGURATION





PART NUMBER INFORMATION

UP8726 AA-BB C	A= Package Code T: TO-252 BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product P: Pb free

ORDERING INFORMATION

Part Number	Package Code	Package	Shipping
UP8726AT-TRG	T	TO-252	2500EA / T&R

※ Year Code : 0~9
※ Week Code : A~Z(1-26); a~z(27~52)
※ G : Green Product. This product is RoHS compliant.

ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25℃	Continuous Drain Current, V_{GS} @ 10V	18	A
I_D @ T_A = 70℃	Continuous Drain Current, V_{GS} @ 10V	14	
I_D @ $T_{C(Bottom)}$ = 25℃	Continuous Drain Current, V_{GS} @ 10V	85	
I_D @ $T_{C(Bottom)}$ = 100℃	Continuous Drain Current, V_{GS} @ 10V	39	
I_D @ T_C = 25℃	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	42	
I_{DM}	Pulsed Drain Current	160	
P_D @T_A = 25℃	Power Dissipation	3.6	W
P_D @$T_{C(Bottom)}$ = 25℃	Power Dissipation	52	
	Linear Derating Factor	0.03	W/℃
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	℃

Note: Absolute maximum ratings are those values bey ond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

ELECTRICAL CHARACTERISTICS (T_A=25℃Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= 250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= 250uA	1.0		2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0			1	uA
		V_{DS}=-24V, V_{GS}=0 T_J=85℃			30	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}= 10V, I_D= 20 A		3.0	4.5	mΩ
		V_{GS}= 4.5V, I_D= 15 A		4.5	6.8	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S= 40 A, V_{GS}=0V		0.7	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS} =15V V_{GS} =10V I_D= 49 A		23		nC
Q_{gs}	Gate-Source Charge			5		
Q_{gd}	Gate-Drain Charge			3		
C_{iss}	Input Capacitance	V_{DS}= 10V V_{GS}=0V f=1MHz		1356		pF
C_{oss}	Output Capacitance			55		
C_{rss}	Reverse Transfer Capacitance			45		
$T_{d(on)}$	Turn-On Time	V_{DS}= 15V I_D= 40A V_{GEN}= 4.5V R_G=1.8		8		nS
T_r				9		
$T_{d(off)}$	Turn-Off Time			32		
T_f				6		

Note: 1. Pulse test: pulse width<=300uS, duty cycle <=2%

2.Static parameters are based on package level with recommended wire bonding

TYPICAL CHARACTERISTICS (25℃ Unless Note)

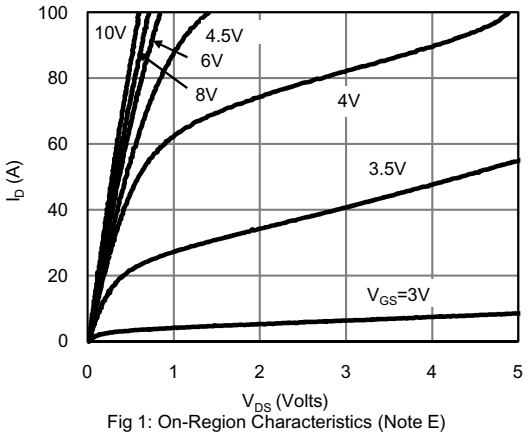


Fig 1: On-Region Characteristics (Note E)

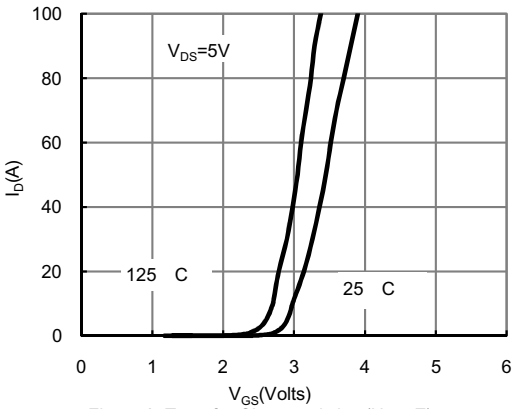


Figure 2: Transfer Characteristics (Note E)

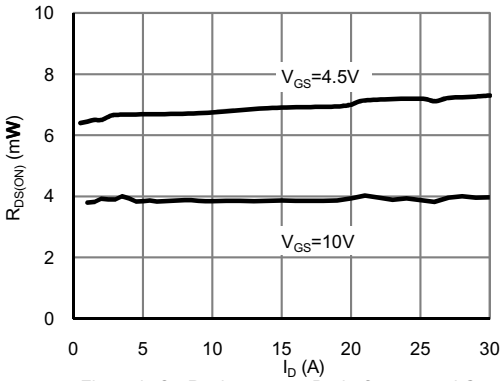


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

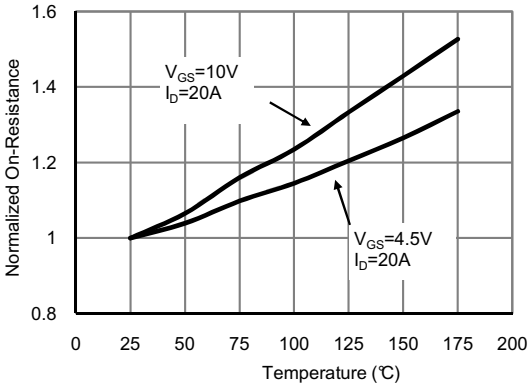


Figure 4: On-Resistance vs. Junction Temperature (Note E)

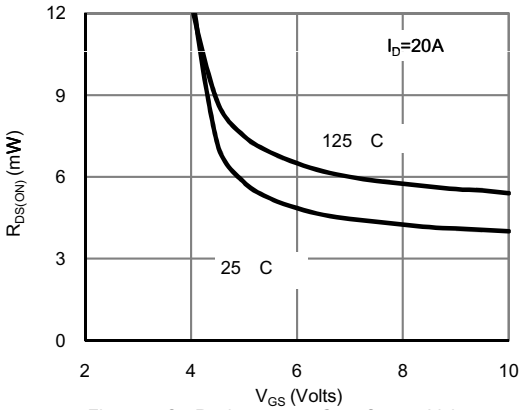


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

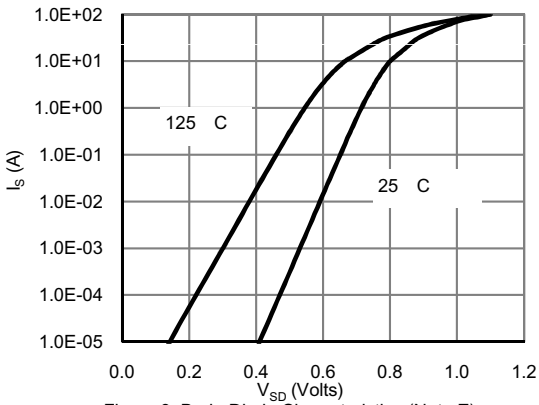


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL CHARACTERISTICS (cont inuous)

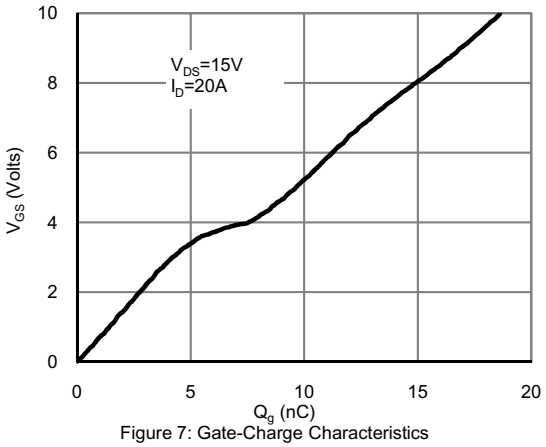


Figure 7: Gate-Charge Characteristics

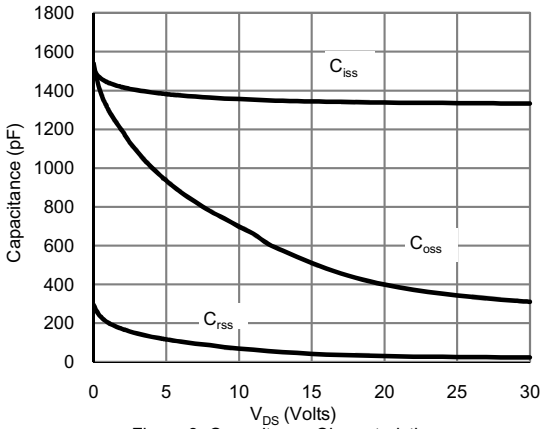


Figure 8: Capacitance Characteristics

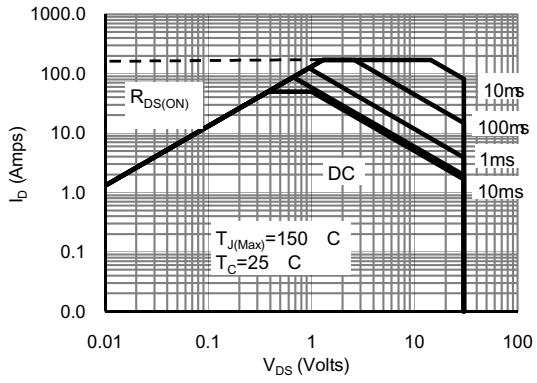


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

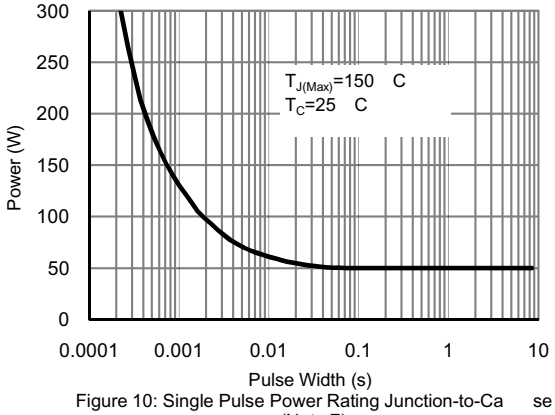


Figure 10: Single Pulse Power Rating Junction-to-Ca se (Note F)

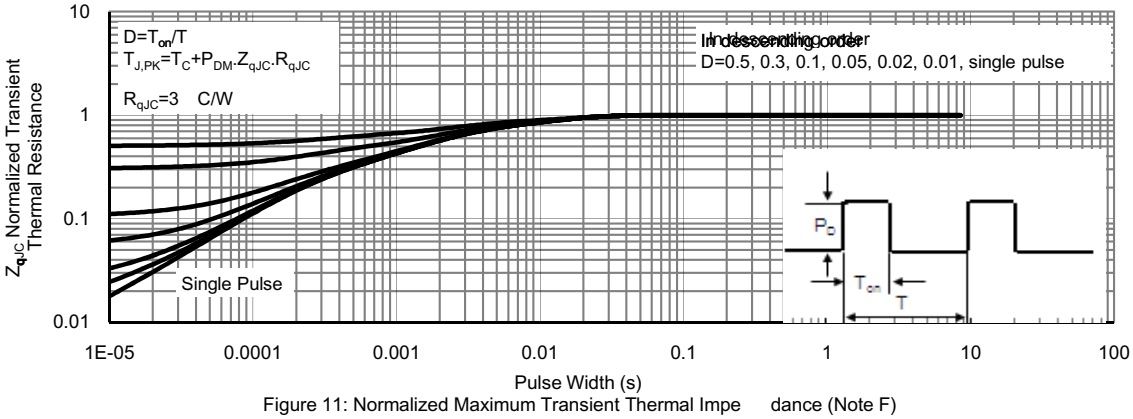
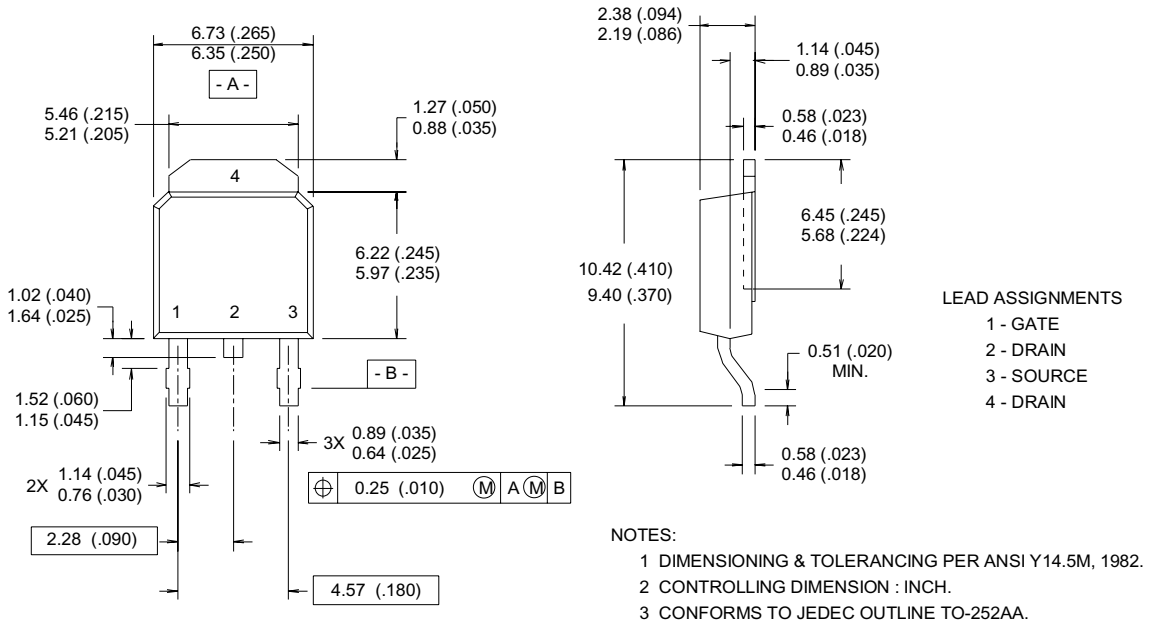


Figure 11: Normalized Maximum Transient Thermal Impe dance (Note F)

TO-252 Outline Package Dimension

θ



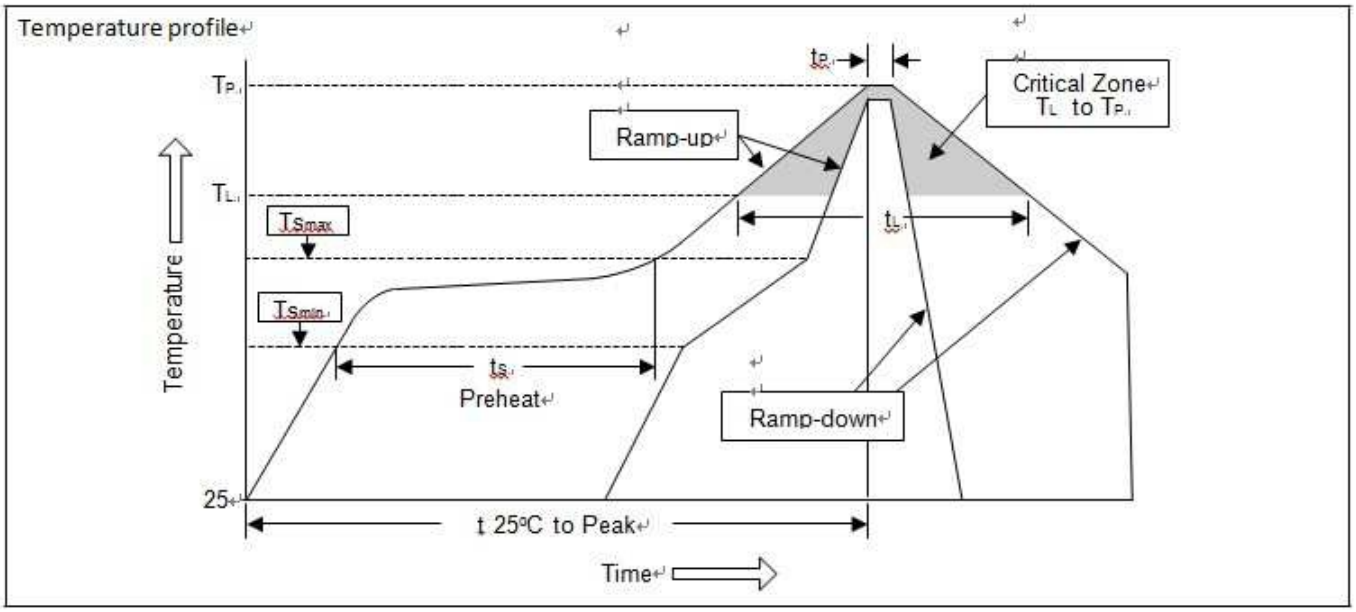
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD Univer Chip Corporation recommends that all integrated cir cuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can causedamage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its pub lished specifications.