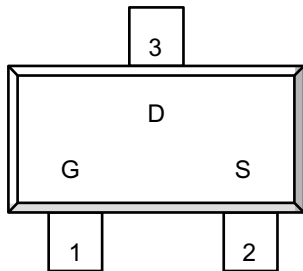


DESCRIPTION

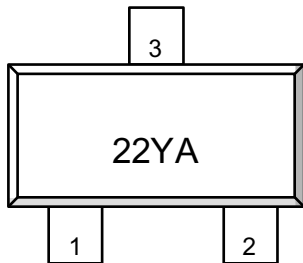
The UP8422A is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This high-density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high side switching.

PIN CONFIGURATION
SOT-23-3L



1.Gate 2.Source 3.Drain

PART MARKING
SOT-23-3L

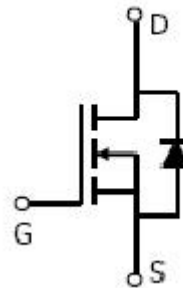


Y: Year Code A: Week Code

FEATURE

- 60V/6.0A, $R_{DS(ON)} = 28m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 60V/2.5A, $R_{DS(ON)} = 38m\Omega$ @ $V_{GS} = 4.5V$
- 60V/1.5A, $R_{DS(ON)} = 100m\Omega$ @ $V_{GS} = 2.5V$

Super high density cell design for extremely low $R_{DS(ON)}$
Exceptional on-resistance and maximum DC current capability
SOT-23-3L package design





ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	I _D	6.0	A
	T _A =25°C		
Pulsed Drain Current	I _{DM}	20	A
Continuous Source Current (Diode Conduction)	I _S	1.7	A
Power Dissipation	P _D	2.0	W
	T _A =25°C		
Operation Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	75	°C/W

6.0A
ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$ $T_J=55^\circ C$			$\frac{1}{10}$	μA
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6.0A$ $V_{GS}=4.5V, I_D=2.5A$ $V_{GS}=2.5V, I_D=1.5A$		28 38 100		m Ω
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=5.8A$		11		S
Diode Forward Voltage	V_{SD}	$I_S=1.7A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V$ $V_{GS}=10V$ $I_D=6.7A$		10	22	nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			3.8		
Input Capacitance	C_{iss}	$V_{DS}=15V$ $V_{GS}=0V$ $F=1MHz$		455		pF
Output Capacitance	C_{oss}			243		
Reverse Transfer Capacitance	C_{rss}			38		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=15V$ $R_L=15\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		8	15	nS
Turn-Off Time	$t_{d(off)}$ t_f			20	40	
				10	20	
				11	20	

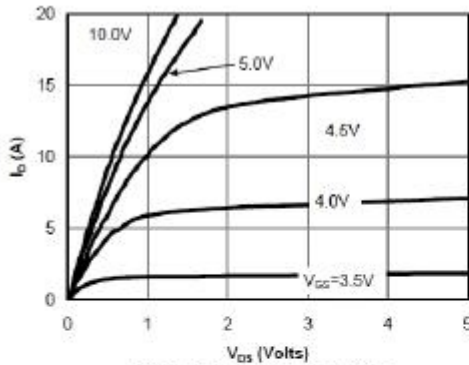
TYPICAL CHARACTERISTICS (25°C Unless noted)


Fig 1: On-Region Characteristics

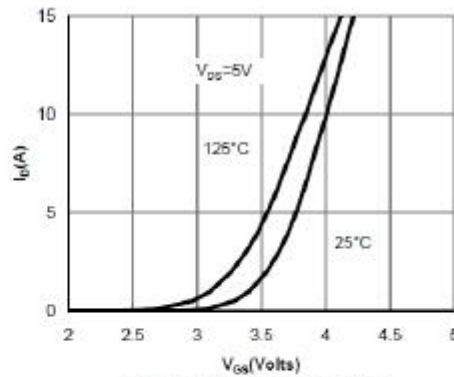


Figure 2: Transfer Characteristics

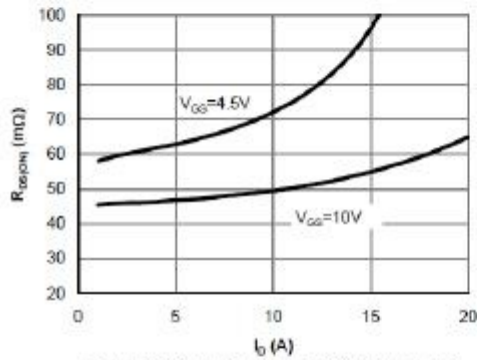


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

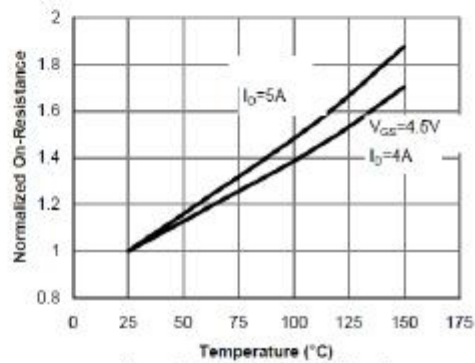


Figure 4: On-Resistance vs. Junction Temperature

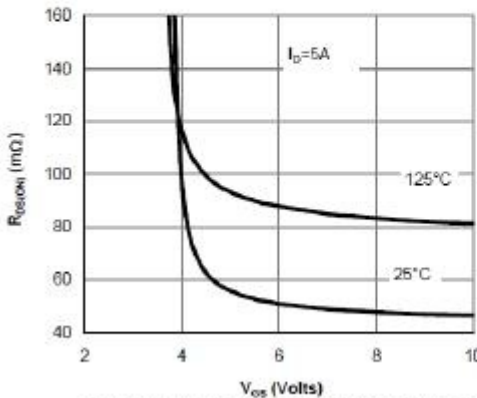


Figure 5: On-Resistance vs. Gate-Source Voltage

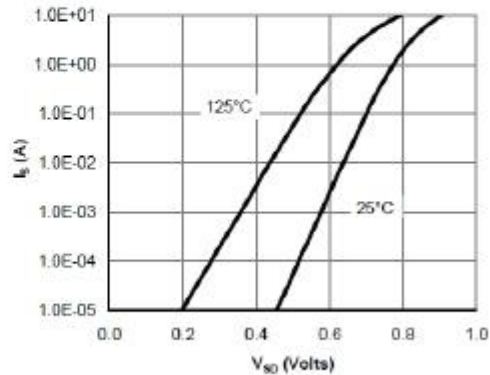


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (25°C Unless noted)

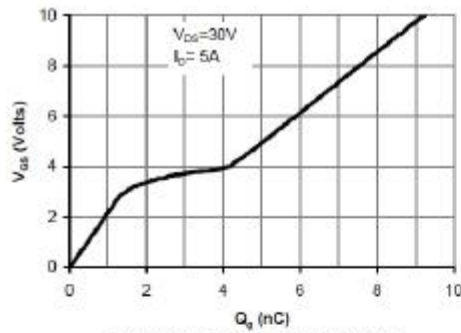


Figure 7: Gate-Charge Characteristics

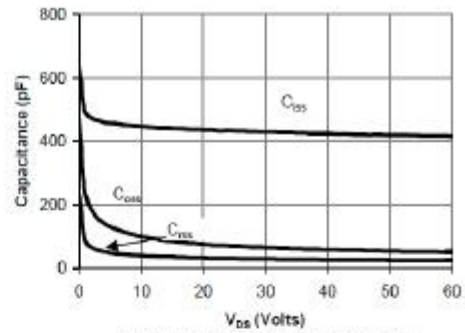


Figure 8: Capacitance Characteristics

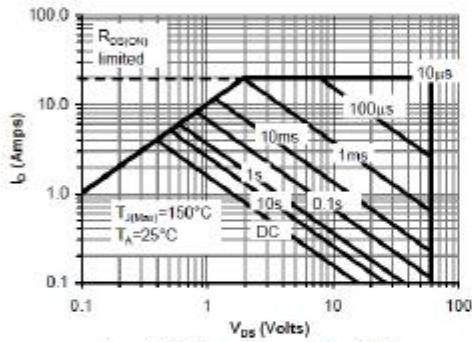


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

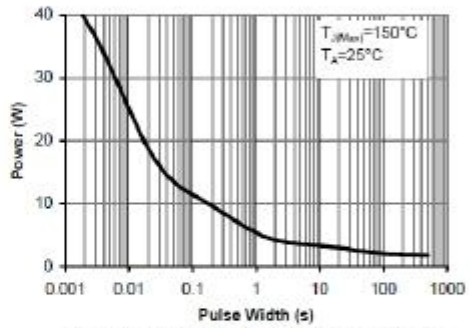


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

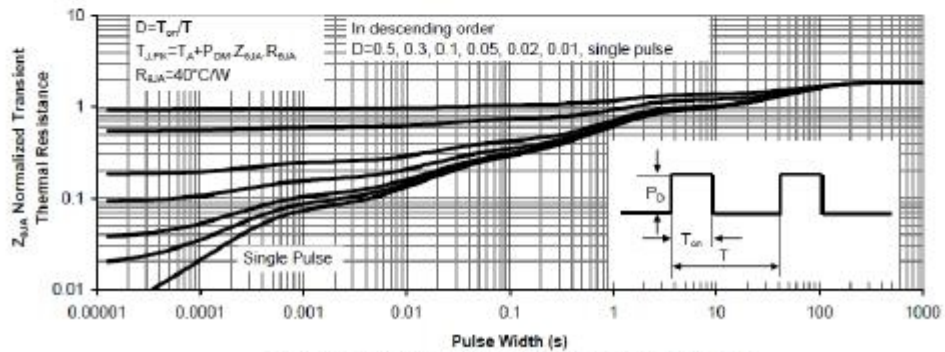
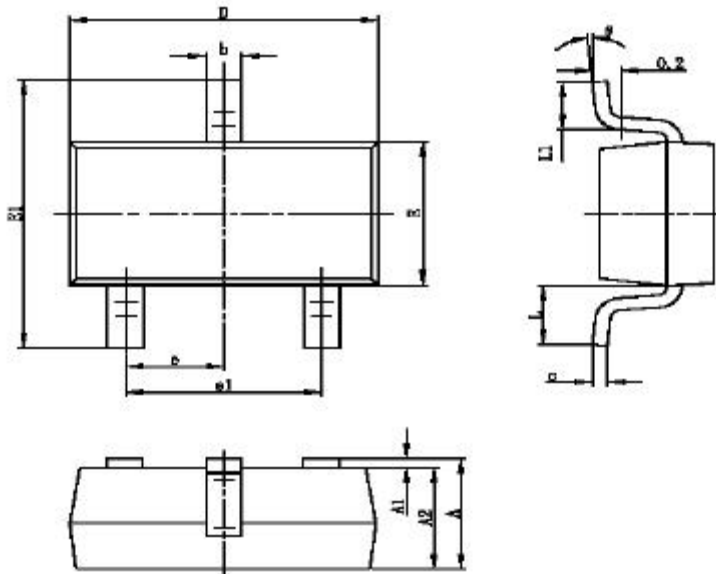


Figure 11: Normalized Maximum Transient Thermal Impedance

6.0A

SOT-23-3L PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°