20V Dual N-Channel Enhancement Mode MOSFET

■ *DESCRIPTION*

The UP8205 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-lin power loss are needed in a very small oupline surface mount package

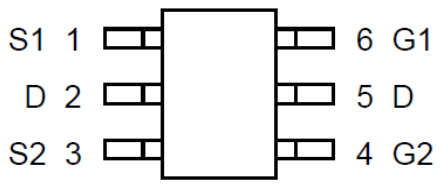
■ *FEATURE*

- ***20V/5.0A, $R_{DS(ON)}$=26mΩ (typ.)@VGS=4.5V***
- ***20V/4.2A, $R_{DS(ON)}$=32mΩ (typ.)@VGS=2.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- This is a Full RoHS compliance
- SOT23-6L TSSOP8 package design

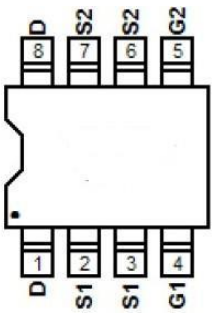
■ *APPLICATIONS*

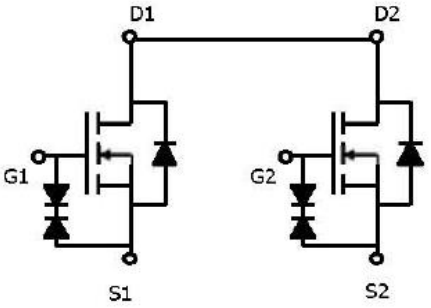
- Power Management in Note Book
- Portable Equipment
- Battery Powered System

■ *PIN CONFIGURATION*



TOP VIEW
SOT-23-6





■ *PART NUMBER INFORMATION*

UP8205AA-BB C	A=Package Code T: TSSOP8 S: SOT23-6L BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
UP8205 AT-TRG	T	TSSOP8	3000EA / T&R
UP8205 AS-TRG	S	SOT23-6L	3000EA / T&R

※ Year Code : 0~9
※ Week Code : A~Z(1-26); a~z(27~52)
※ G : Green Product. This product is RoHS compliant.

■ ABSOLUPE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical		Unit
V_{DSS}	Drain-Source Voltage		-20		V
V_{GSS}	Gate-Source Voltage		±12		V
I_D	Continuous Drain Current (TJ=150℃)	VGS-4.5V	5		A
I_{DM}	Pulsed Drain Current		20		A
I_S	Continuous Source Current (Diode Conduction)		1		A
P_D	Power Dissipation	TA=25℃	1.25(SOT23-6L)	1.5(TSSOP8)	W
		TA=75℃	0.8(SOT23-6L)	1(TSSOP8)	
T_J	Operation Junction Temperature		150		℃
T_{STG}	Storage Temperature Range		-55~+150		℃

Note: Absolupe maximum ratings are those values beyond which the device could be permanently damaged. Absolupe maximum ratings are stress rating only and functional device operation is not implied

■ THERMAL DATA

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5	125	℃/W

■ *ELECTRICAL CHARACTERISTICS(VDD=2.75V, T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.5		1	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0			1	uA
		V_{DS}=16V, V_{GS}=0 T_J=85℃			30	
$I_{D(ON)}$	On=State Drain Current	V_{DS}≧5V, V_{GS}=4.5V	6			A
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=4.5V, I_D=4A		26	32	mΩ
		V_{GS}=2.5V, I_D=3A		32	38	
		V_{GS}=1.8V, I_D=3A		35	40	
G_{fs}	Forward Transconductance	V_{DS}=5V, I_D=3.6A		10		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.8	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=10V V_{GS}=4.5V I_D=6A		21	29	nC
Q_{gs}	Gate-Source Charge			1.3		
Q_{gd}	Gate-Drain Charge			3.3		
C_{iss}	Inpup Capacitance	V_{DS}=10V V_{GS}=0V f=1MHz		595		pF
C_{oss}	Ouppup Capacitance			140		
C_{rss}	Reverse Transfer Capacitance			125		
$T_{d(on)}$	Turn-On Time	V_{DS}=10V R_L=10Ω I_D=1A V_{GEN}=4.5V R_G=6Ω		3.6	7	nS
T_r				13.5	25	
$T_{d(off)}$	Turn-Off Time			32	58	
T_f				6.6	13	

Note: 1. Pulse test: pulse width<=300uS, dupy cycle<=2%

2.Static parameters are based on package level with recommended wire bonding